REMARKS

Applicants appreciate the examination of the present application, which is evidenced by the Official Action of March 22, 2005. In response to the examination, Applicants have amended independent Claims 1, 9, 13 and 17 and dependent Claim 2. Based on these amendments, Applicants respectfully submit the present application is in condition for allowance.

The Pending Claims are Patentable Over Hamade et al.

Applicants acknowledge that FIGS. 21 and 27 of Hamade et al. disclose a plurality of sense amplifier block portions, which are designated by the reference characters b0-b32. (See also, Hamade et al., Col. 15, lines 43-44). These sense amplifier block portions b0-b32 extend between corresponding ones of the memory blocks #0, ..., #32. In this regard, the disclosure at FIG. 21 of Hamade et al. is essentially identical to the admitted prior art at FIG. 2 of the present application. However, the disclosure of Hamade et al. provides absolutely no suggestion of the subject matter of the pending claims. For example, Claim 1, as amended, recites:

> 1. (Currently amended) An integrated circuit memory device, comprising:
> first and second memory blocks; and
> a sense amplifier array **[[**that is**]]** extending between and electrically coupled to said first and second memory blocks by first and second pluralities of pairs of bit lines, respectively, said sense amplifier array having first and second column select I/O blocks therein **[[**that are**]]** arranged in an alternating zig-zag layout sequence that extends between immediately opposing sides of said first and second memory blocks.

This Claim 1 covers the embodiment of FIG. 4A of the present application. As illustrated by the zero sense amplifier region (SAR0) on the left side of FIG. 4A, the column select I/O blocks are arranged in an zig-zag layout sequence across the first and second rows of the sense amplifier array. This sense amplifier array and the zig-zag layout sequence of column select I/O blocks therein extends

between immediately adjacent memory blocks MB0 and MB1. This zig-zag layout sequence of FIG. 4A is in stark contrast to the separate layout arrangements of the separated sense amplifier block portions b1 and b2 illustrated by FIG. 21 of Hamade et al., which do not extend between immediately opposing sides of adjacent memory blocks. Instead, the sense amplifier block portion b1 of FIG. 21 extends between memory block #0 and memory block #1 and the sense amplifier block portion b2 extends between memory block #1 and memory block #2. Neither of these sense amplifier block portions (b0, b1, b2, ..., b32) contains a zig-zag layout sequence of column select I/O blocks. Applicants respectfully submit, therefore, that Hamade et al. does not disclose or suggest the subject matter of Claim 1 of the present application. This same argument also applies to independent Claim 9.

Moreover, with respect to independent Claim 13, FIG. 4B of the present application illustrates a first column-to-I/O control block (including blocks 140 and 150) connected to a first pair of sense bit lines SBL0 and SBL0B and a second column-to-I/O control block (including blocks 140 and 150) connected to a second pair of sense bit lines SBL2 and SBL2B. These first and second column-to-I/O control blocks are recited as being immediately adjacent to each other. Claim 13 also recites that the second column select I/O block 150 (associated with SBL2/SBL2B) extends opposite the first N-type (P-type) sense amplifier block 140 (associated with SBL0/SBL0B) and the second N-type (P-type) sense amplifier block 140 (associated with SBL2/SBL2B) extends opposite the first column select I/O block 150 (associated with SBL0/SBL0B). Because these aspects of Claim 13 are not disclosed or suggested by Hamade et al., Applicants respectfully submit that Claim 13 is patentable. Amended Claim 17 is also patentable for similar reasons.

Finally, although not addressed specifically by the Examiner, the subject matter of independent Claim 19 of the present application, which recites "eight column selection transistors having gate terminals that are electrically connected together by a common polysilicon gate line," is not disclosed or suggested by Hamade et al. The same is true for independent Claim 15, which recites a unit cell layout structure containing four quadrants with different blocks therein. This type of layout structure is not disclosed or suggested by Hamade et al.

Applicants have shown that Hamade et al. does not disclose or suggest the subject matter of the pending independent claims. Accordingly, Applicants submit that the present application is in condition for allowance.

Respectfully submitted,

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